Modeling of RF Energy Scavenging for Batteryless Wireless Sensors with Low Input Power

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***Abstract*—RF energy scavenging enables batteryless operation of wireless sensors. In particular, a system with a central controller that transfers wireless energy to and exchanges information with RF energy scavenging sensors is very suitable for a wide range of applications. State-of-the-art analysis of RF energy scavenging is mostly based on RF-DC rectifier models operating with relatively high input power to achieve high rectification efficiency. However, to enable larger distance between the central controller and sensors and/or to increase the operating frequencies, which can lead to small and low-cost smart dust like sensors, a good model describing the RF-DC rectification with low input power is needed to aid system design and optimization. In this paper, we develop such a model. Using the model, we derive closed-form solutions for the equilibrium voltage and the input resistance of the rectifier. We further propose a quasi-static model to describe the dynamic charging of the capacitor in the rectifier. A comparison with circuit simulations using Cadence Virtuoso Spectre circuit simulator shows good match between our model the circuit simulation.**

I. Introduction

Energy scavenging enables batteryless operation of wireless sensors. Since wireless sensors use wireless/RF signals for communication, it is a natural choice to utilize RF energy scavenging from dedicated wireless power transfer. The radio frequency identification (RFID) system is a typical example that combines wireless signal transmission with RF energy scavenging. The design of intelligent ultra-low power, self-powering wireless sensors requires innovative circuit designs that stretch the limits of current designs and models. Hitherto, most designs and performance evaluations relied on computer-intensive numerical simulators. Tractable models that allow system design and optimization have not been fully developed. This is partly due to the nonlinear nature of the RF-DC rectification, which is a very critical part of RF energy scavenging. Previous studies on RF-DC rectification mainly focus on the high rectifier input power regime to achieve high rectification efficiency [1]. Already, we have seen studies on μ-power rectifiers with lower input power resulting in available voltage near diodes' threshold voltages [2]. As we further extend the operation range and/or increase the operating frequency to the millimeter wave bands, which enables low-cost and small (even fully monolithic) sensors [3], the study of RF energy scavenging in a very low input power regime becomes relevant and essential.

In this paper, for RF energy scavenging in the very low input power regime, we make a first attempt to develop a model that is very suitable for system-level performance evaluation and optimization of ultra-low power, RF scavenging sensor nodes. This paper shows that key parameters, not only the steady-state equilibrium voltage but also the charge-dependent variations in the rate energy built-up or input impedance can be expressed in terms of Bessel functions, which have well-studied mathematical properties. Moreover, we use the Cadence Virtuoso Spectre circuit simulator, which is widely used among IC designers for simulating RFIC circuits, to validate our model. A good match is achieved between our model and the circuit simulation.

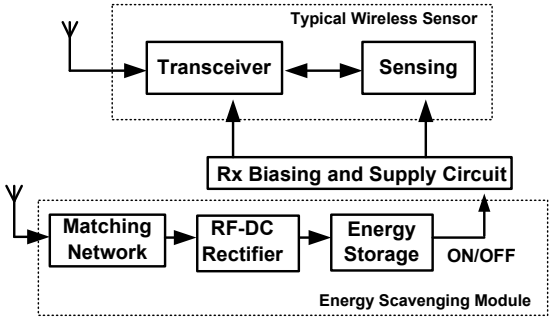

Fig. 1. Block diagram of a wireless sensor with RF energy scavenging.

The rest of this paper is organized as follows. In Section II, we describe the wireless sensor with RF energy scavenging and the relevance of the study with low input power. The model of low input power RF-DC rectification is developed in Section III and comparisons with circuit simulation results are given in Section IV. The concluding remarks are drawn in Section V.

II. Wireless sensors with RF Energy Scavenging

Figure 1 shows a block diagram of a wireless sensor with RF energy scavenging. It includes a typical wireless sensor with a sensing module and a transceiver for communication. The energy required for the wireless sensor is provided by an energy scavenging module that receives RF energy via wireless power transfer, converts it to DC and stores the DC energy in the energy storage. In the energy scavenging module, the RF energy is received from a receive antenna and a matching network is used to ensure maximum power transfer from the antenna to the rest of the circuit. A very critical part of the energy scavenging module is the RF-DC rectifier, which converts the RF energy to DC suitable for storage in the energy storage.

One key parameter that affects the efficiency of the RF-DC rectifier is the voltage V_{in} at the rectifier input. This is

Parameters	2.4 GHz RFID	60 GHz
P_{T} (dBm)	20	20
G_{T} (dB)	11	20
G_{R} (dB)	0	0
η_{a}	0.9	0.6
η_{m}	0.75	0.7

TABLE I
SYSTEM PARAMETERS FOR THE EXAMPLE 2.4 GHZ AND 60 GHZ BATTERYLESS WIRELESS SENSORS

directly related to the power P_{in} available at the rectifier input, determined by

$$P_{\mathrm{in}} = \frac{P_{\mathrm{T}} G_{\mathrm{T}} G_{\mathrm{R}}}{L_{\mathrm{P}}} \eta_{\mathrm{a}} \eta_{\mathrm{m}}, \tag{1}$$

where P_{T} is the transmit power from the central controller transmitter, G_{T} is the transmit antenna gain and G_{R} is the receive antenna gain at the sensor node. The free space propagation loss L_{P} is given by $L_{\mathrm{P}} = \left(\frac{4\pi df}{c_o}\right)^2$, where d is distance between the central controller and the sensor, f is the frequency and $c_o = 3 \times 10^8$ m/s is the speed of light. We use η_{a} to denote the receive antenna efficiency and η_{m} to denote the efficiency of the matching network. For frequencies in the order of a few GHz, these two factors are close to 1 with properly designed antenna and matching network. For millimeter-wave applications, it is possible to integrate receive antenna on chip and thus have a fully monolithic sensor node [3] [4]. In this case, due to the monolithic constraint, both η_{a} and η_{m} are lower compared to low frequency applications. Figure 2 shows a typical example of P_{in} for both 2.4 GHz RFID and 60 GHz applications. The system parameter values used in the calculations are listed in Table I. The matching efficiency of the 2.4 GHz RFID system is 0.75 due to the mismatch required for backscatter modulation used in RFID. We can see that for the 2.4 GHz system, extending the range to about 10 m will reduce the rectifier input power below -30 dBm. This results in an input voltage in the order of 100 mV. This value is below the threshold voltage of typical diodes and is in the subthreshold operation region. For the shown 60 GHz system, the study of subthreshold RF-DC rectification is even more relevant due to the low rectifier input power resulting mainly from large path loss.

III. MODELING OF RF-DC RECTIFICATION WITH LOW INPUT POWERS

The RF-DC voltage rectifier is normally implemented as connected N single-stage rectifiers each with a capacitor and a diode. If all the N stages use the same capacitors and diodes, the performance of the N-stage rectifier can be characterized with good approximation by the performance of a single stage rectifier [1] [5]. As a result, in the rest of the paper, we focus our study on a single-stage rectifier as shown in Figure 3. The input is a sinusoidal voltage source with amplitude V_{A} and frequency ω. The diode can be a junction diode, or a diode-connected MOS transistor and C_{load} is the storage capacitor.

Using a SPICE model for the diode [6], which is also

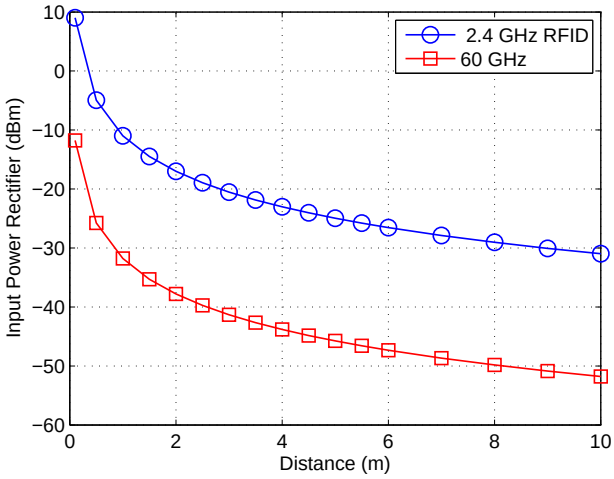

Fig. 2. Receive power available at the rectifier input.

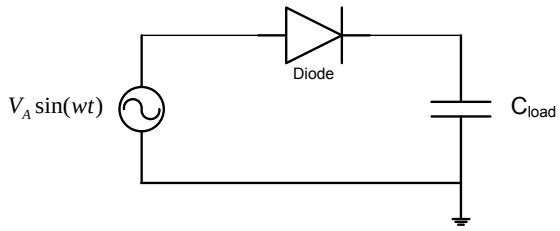

Fig. 3. Single stage Rectifier Structure.

a good approximation for diode-connected MOS transistor for subthreshold regions [1], the equivalent small signal (AC signal) model for the single stage rectifier is depicted in Figure 4. In the small signal model, a practical diode is modeled as four components, namely an ideal diode, a series resistance R_{se} that models ohmic resistance from the diode, a parallel capacitance C_{par} that models the parasitic junction capacitances and a shunt resistance R_{sh}. The shunt resistance is included in the SPICE model to aid convergence in the numerical calculations and has a default value of $10^{12}\Omega$ [6]. It is thus not necessary in the analytical model that we are developing. However, in our model, we include R_{sh} to account

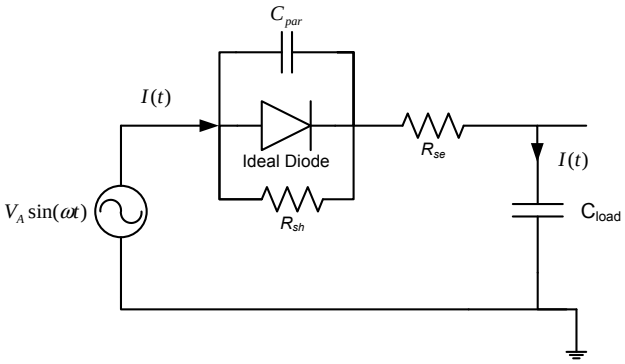

Fig. 4. Small signal model of the single stage rectifier.

for the additional leakage current in the reversed bias region of a practical diode. In the following, we are going to develop analytical models for two cases both without and with R_{sh}.

The current through an ideal diode due to a time varying voltage $V_{\text{d}}(t)$ is given by [6]

$$I_{\text{d}}(t) = I_{\text{s}} \left(\exp\left(\frac{V_{\text{d}}(t)}{N V_{\text{T}}} \right) - 1 \right), \tag{2}$$

where I_{s} is the saturation current, V_{T} is the thermal voltage and N is the ideality factor. The thermal voltage is given by $V_{\text{T}} = \frac{kT}{q} \approx 26$ mV at room temperature ($T \approx 300K$) and N has a value close to 1. The parasitic capacitance has a voltage dependent capacitance value given by

$$C_{\text{par}}(t) = C_0 \left(1 - \frac{V_{\text{d}}(t)}{V_0} \right)^{-0.5}, \tag{3}$$

where C_0 is the zero bias junction capacitance and V_0 is the contact potential having a typical value of 0.6 to 0.8 V. The current through C_{par} can thus be written as

$$I_{\text{c}}(t) = \frac{d(C_{\text{par}}(t) V_{\text{d}}(t))}{dt} = C_{\text{par}(t)} \frac{\partial V_{\text{d}}(t)}{\partial t} + V(t) \frac{\partial C_{\text{par}}(t)}{\partial t}. \tag{4}$$

The current through R_{sh} is given by

$$I_{\text{R}}(t) = \frac{V_{\text{d}}(t)}{R_{\text{sh}}}, \tag{5}$$

and the total current $I(t) = I_{\text{d}}(t) + I_{\text{c}}(t) + I_{\text{R}}(t)$. The net electric charge accumulated on the storage capacitance in a charging cycle is thus given by

$$\Delta Q = \int_{t=0}^{T} I_{\text{d}}(t) dt + \int_{t=0}^{T} I_{\text{c}}(t) dt + \int_{t=0}^{T} I_{\text{R}}(t) dt, \tag{6}$$

where $T = 1/(\omega/(2\pi))$ is the period of the RF charging signal. For the case where we do not consider R_{sh}, $R_{\text{sh}} = \infty$ and $I_{\text{R}}(t) = 0$ in (6).

In the subsequent analysis, we make the following key assumptions

1) The storage capacitance is large enough such that the voltage across the capacitance V_c in one charging cycle T is constant.
2) The voltage drop on R_{se} is negligible and we have $V_{\text{d}}(t) = V_{\text{A}} \sin(\omega t) - V_{\text{c}}$, where V_{c} is the voltage across C_{load}. This is because the series resistance R_{se} is in the order of tens of Ω and is very small compared to the equivalent impedance of the other three components. This assumption holds well when the maximum forward bias voltage is in the subthreshold region and the frequency is below 5 GHz.

A. Equilibrium voltage

Using (2), we get

$$\begin{aligned} \int_0^T I_{\text{d}}(t) dt &= \int_0^T I_{\text{s}} \left(\exp\left(\frac{V_{\text{A}} \sin(\omega t) - V_{\text{c}}}{N V_{\text{T}}} \right) - 1 \right) dt \\ &= I_{\text{s}} T \left(\exp\left(-\frac{V_{\text{c}}}{N V_{\text{T}}} \right) \mathcal{I}_0 \left(\frac{V_{\text{A}}}{N V_{\text{T}}} \right) - 1 \right), \end{aligned} \tag{7}$$

The appearance of the modified Bessel function $\mathcal{I}_0(x)$ of the first kind and order 0 was recognized by Harison [7] in his analysis of analog TV reception. Because of symmetry properties over one sinusoidal cycle in (4), it can be shown that $\int_{t=0}^{T} I_{\text{c}}(t) dt = 0$. In the steady state of the rectifier, the electric charges that enter C_{load} should be equal to the electric charges leaving it. Therefore, $\Delta Q = 0$ for one charging cycle. As a result, without considering R_{sh}, from (7), we have

$$\left(\exp\left(-\frac{\widetilde{V_{\text{c}}}}{N V_{\text{T}}} \right) \mathcal{I}_0 \left(\frac{V_{\text{A}}}{N V_{\text{T}}} \right) - 1 \right) = 0,$$

where $\widetilde{V_{\text{c}}}$ is the equilibrium voltage, and

$$\widetilde{V_{\text{c}}} = N V_{\text{T}} \log\left(\mathcal{I}_0 \left(\frac{V_{\text{A}}}{V_{\text{T}}} \right) \right). \tag{8}$$

Previous studies on scavenging rectifiers relied on numerical methods to evaluate V_{c} [1] [2]. The Bessel function $\mathcal{I}_0$ allows us to phrase V_{c} as the analytical expression (8) and also appears instrumental for further evaluation. Expression (8) is valid for weak RF signals that keep the diode in the subthreshold regime. In fact, a first-order Taylor's series approximation of the Bessel function yields $V_{\text{c}} \approx \frac{V_{\text{A}}^2}{4 N V_{\text{T}}}$ and confirms the highly non-linear behavior between the rectifier input voltage and equilibrium voltage that poses design challenges.

To include R_{sh}, we also need to consider the electric charge goes through it. Using (5), we get

$$\int_{t=0}^{T} I_{\text{R}}(t) dt = -\frac{V_c}{R_{\text{sh}}} T. \tag{9}$$

Again, when $\Delta Q = 0$, we have

$$I_{\text{s}} \left(\exp\left(-\frac{\widetilde{V_{\text{c}}^{\text{R}}}}{N V_{\text{T}}} \right) \mathcal{I}_0 \left(\frac{V_{\text{A}}}{N V_{\text{T}}} \right) \right) - \left(I_{\text{s}} + \frac{V_c^{\text{R}}}{R_{\text{sh}}} \right) = 0, \tag{10}$$

and the equilibrium voltage $\widetilde{V_{\text{c}}^{\text{R}}}$, considering R_{sh}, can be obtained numerically. From (10), we get

$$\widetilde{V_{\text{c}}^{\text{R}}} = N V_{\text{T}} \log\left(\mathcal{I}_0 \left(\frac{V_{\text{A}}}{N V_{\text{T}}} \right) \right) - N V_{\text{T}} \log\left(1 + \frac{\widetilde{V_{\text{c}}^{\text{R}}}}{I_{\text{s}} R_{\text{sh}}} \right). \tag{11}$$

For $\frac{\widetilde{V_{\text{c}}^{\text{R}}}}{I_{\text{s}} R_{\text{sh}}} << 1$, using Taylor's series approximation, $\log\left(1 + \frac{\widetilde{V_{\text{c}}^{\text{R}}}}{I_{\text{s}} R_{\text{sh}}} \right) \approx \frac{\widetilde{V_{\text{c}}^{\text{R}}}}{I_{\text{s}} R_{\text{sh}}}$ and we can obtain the closed-form approximation for the equilibrium voltage as

$$\widetilde{V_{\text{c}}^{\text{R}}} \approx \frac{N V_{\text{T}} \log\left(\mathcal{I}_0 \left(\frac{V_{\text{A}}}{N V_{\text{T}}} \right) \right)}{1 + \frac{N V_{\text{T}}}{I_{\text{s}} R_{sh}}}. \tag{12}$$

Comparing (12) with (8), we can see that including R_{sh} results in a smaller equilibrium voltage. The effect of R_{sh} shows on the additional term $\frac{N V_{\text{T}}}{I_{\text{s}} R_{sh}}$ in the denominator that accounts for the additional leakage current through R_{sh} in the reversed-bias region.

B. Input resistance

The input resistance is an important parameter for designing the matching network that maximizes power transfer from the

antenna to the rectifier. Due to the nonlinear current through the diode, the input resistance is no longer a constant [2]. In this section, we determine an average input resistance $\overline{R_{\text{in}}}$ related to the mean power that enters the rectifier in one charging cycle [2]

$$\begin{aligned}\overline{P_{\text{in}}} &= \frac{1}{T}\int_0^T V_{\text{A}}\sin(\omega t)I(t)dt \\ &= \frac{1}{T}\int_0^T V_{\text{A}}\sin(\omega t)(I_{\text{d}}(t)+I_{\text{c}}(t)+I_{\text{R}}(t))dt.\end{aligned} \tag{13}$$

Using (2), we get

$$\begin{aligned}&\frac{1}{T}\int_0^T V_{\text{A}}\sin(\omega t)I_{\text{d}}(t)dt \\ =\ &\frac{1}{T}\int_0^T V_{\text{A}}I_{\text{s}}\left(\exp\left(\frac{V_{\text{d}}(t)}{NV_{\text{T}}}\right)-1\right)\sin(\omega t)dt \\ =\ &V_{\text{A}}I_{\text{s}}\exp\left(-\frac{V_{\text{c}}}{NV_{\text{T}}}\right)\mathcal{I}_1\left(\frac{V_{\text{A}}}{NV_{\text{T}}}\right) \\ =\ &V_{\text{A}}I_{\text{s}}\frac{\mathcal{I}_1\left(\frac{V_{\text{A}}}{NV_{\text{T}}}\right)}{\mathcal{I}_0\left(\frac{V_{\text{A}}}{NV_{\text{T}}}\right)},\end{aligned} \tag{14}$$

where $\mathcal{I}_1(x)$ is the modified Bessel function of the first kind and order 1. Using (4), it can be shown that $\frac{1}{T}\int_0^T V_{\text{A}}\sin(\omega t)I_{\text{c}}(t)dt = 0$. As a result, without considering R_{sh}, we have

$$\overline{P_{\text{in}}} = V_{\text{A}}I_{\text{s}}\frac{\mathcal{I}_1\left(\frac{V_{\text{A}}}{NV_{\text{T}}}\right)}{\mathcal{I}_0\left(\frac{V_{\text{A}}}{NV_{\text{T}}}\right)}, \tag{15}$$

and the average input resistance over a charging cycle

$$\overline{R_{\text{in}}} = \frac{1}{2}\frac{V_{\text{A}}^2}{\overline{P_{\text{in}}}} = \frac{V_{\text{A}}}{2I_{\text{s}}}\frac{\mathcal{I}_0\left(\frac{V_{\text{A}}}{NV_{\text{T}}}\right)}{\mathcal{I}_1\left(\frac{V_{\text{A}}}{NV_{\text{T}}}\right)}. \tag{16}$$

When considering R_{sh}, using (5), we get

$$\frac{1}{T}\int_0^T V_{\text{A}}\sin(\omega t)I_{\text{R}}(t)dt = \frac{V_{\text{A}}^2}{2R_{\text{sh}}}, \tag{17}$$

and

$$\overline{P_{\text{in}}} = V_{\text{A}}I_{\text{s}}\exp\left(-\frac{V_{\text{c}}^{\text{R}}}{NV_{\text{T}}}\right)\mathcal{I}_1\left(\frac{V_{\text{A}}}{NV_{\text{T}}}\right)+\frac{V_{\text{A}}^2}{2R_{\text{sh}}}. \tag{18}$$

The average input resistance in this case is equal to

$$\overline{R_{\text{in}}^{\text{R}}} = \frac{1}{\frac{2I_{\text{s}}\exp\left(-\frac{\widetilde{V_{\text{c}}^{\text{R}}}}{NV_{\text{T}}}\right)\mathcal{I}_0\left(\frac{V_{\text{A}}}{NV_{\text{T}}}\right)}{V_{\text{A}}}+\frac{1}{R_{\text{sh}}}}. \tag{19}$$

To get more insight from (19), we assume $\widetilde{V_{\text{c}}^{\text{R}}} \approx \widetilde{V_{\text{c}}}$, then

$$\overline{R_{\text{in}}^{\text{R}}} \approx \frac{1}{\frac{1}{\overline{R_{\text{in}}}}+\frac{1}{R_{\text{sh}}}}. \tag{20}$$

and this is the equivalent resistant of a parallel-connected $\overline{R_{\text{in}}}$ as in (16) and R_{sh}.

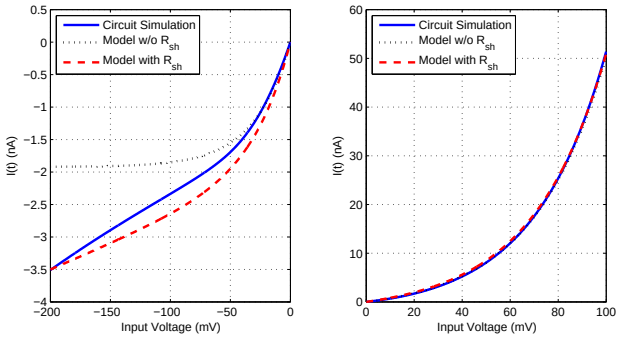

Fig. 5. Comparison of the model and circuit simulator - DC performance.

C. Charging of the storage capacitor

To be able to describe the charging of C_{load} over time, we propose a quasi-static charging model. We assume that the voltage on C_{load} stays constant within T, while the voltage increment from nT to $(n+1)T$ is given by

$$\begin{aligned}V((n+1)T)-V(nT) &= \frac{\int_{t=nT}^{(n+1)T} I(t)dt}{C_{\text{load}}} \\ &= \frac{T}{C_{\text{load}}}\left(I_{\text{s}}\left(\exp\left(-\frac{V(nT)}{NV_{\text{T}}}\right)\mathcal{I}_0\left(\frac{V_{\text{A}}}{NV_{\text{T}}}\right)-1\right)-\frac{V(nT)}{R_{\text{sh}}}\right),\end{aligned} \tag{21}$$

and with this, we can determine the voltage on the capacitor in a given time period. Similarly, we can obtain that the energy accumulated during one charging cycle is given by

$$E((n+1)T)-E(nT) = \frac{1}{2}C_{\text{load}}\left(V^2((n+1)T)-V^2(nT)\right), \tag{22}$$

while the power scavenges is given by

$$P(nT) = \frac{1}{2T}C_{\text{load}}\left(V^2((n+1)T)-V^2(nT)\right). \tag{23}$$

IV. Comparison with Circuit Simulation Results

In this section, we compare the performance of the one-stage rectifier calculated using our model with that obtained using the Cadence Virtuoso Spectre circuit simulator. In the circuit simulation, we use a diode connected NMOS field effect transistor (FET) in CMOS 65nm technology. The NMOS FET used in the simulator has a channel length of 60 nm, a channel width of $2\mu m$ and has 3 fingers. The diode parameters used in the model are listed in Table II. Firstly, we compare the DC performance of the diode-connected transistor. Figure 5 shows the DC current through the diode as a function of the DC voltage for the reverse biased and forward biased (subthreshold) regions obtained using the model and the circuit simulator. In the forward biased region, our model agrees well with circuit simulator. In the reverse bias region, without using the shunt resistance, the DC (leakage) current obtained using the model is too small compared to that obtained using the circuit simulator. With the shunt resistance, the current becomes similar.

Figure 6 shows the voltage charged on C_{load} obtained using the quasi-static charging model (21) and using the Cadence circuit simulator. We also plotted two equilibrium voltage values obtained using (12) and (8) with and without

Parameters	Values
I_s	1.922 nA
R_{sh}	126.4 MΩ
V_T	26 mV
N	1.15
C_0	7 fF
V_0	0.6 V
C_{load}	1 pF
f	2 GHz
V_A	100 mV

TABLE II
DIODE PARAMETERS USED IN THE MODEL.

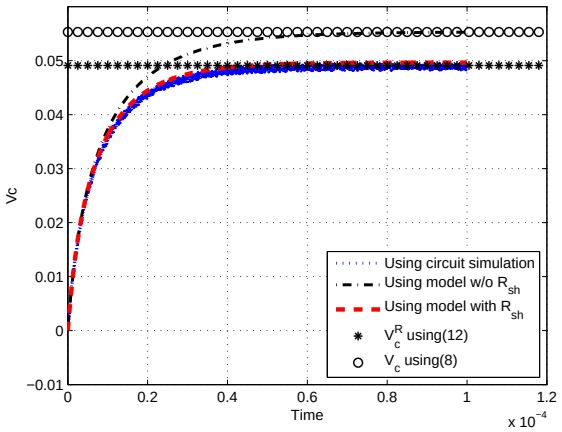

Fig. 6. Comparison of capacitor charging performance using the model and circuit simulator.

R_{sh}. Without considering R_{sh}, the diode leakage current in the reverse-bias case is smaller than that using the circuit simulator. As a result, the equilibrium voltage obtained from our model (8) appears to be higher than that from the circuit simulator. The addition of R_{sh} improves the match between the final equilibrium voltage predicted by the developed model (12) and obtained from the circuit simulator. Moreover, the charging of capacitor over time obtained from the quasi-static model matches closely with the circuit simulator result.

From Figure 6, we can see that initially, the voltage grows linearly, thus the energy as shown in (22) grows quadratically with time. As a result, the power scavenges as shown in (23) grows also linearly with time. After certain time, due to the accumulated voltage on C_{load}, the voltage built up becomes slow and eventually reaches the equilibrium. After this moment further scavenging is much less effective and the system should switch to sensing and transmission modes. Therefore, as an example, the developed model is very useful in designing a communication and energy scavenging protocol that achieves optimal division between energy scavenging and communication.

The equilibrium voltage for a single-stage rectifier is about 50 mV as shown in Figure 6. Cascading 20 stages in a practical rectifier will result in a DC voltage of about 1V. Considering a practical on-chip storage capacitor size of 1nF [4], the energy scavenged is about 0.5 nJ, which is sufficient to power a fully monolithic 60 GHz wireless sensor node for close-range short-packet communication [8].

V. CONCLUSIONS

In this paper, we developed a model for RF energy scavenging under low input power regime. We show that key parameters such as equilibrium voltage and input resistance, can be described in terms of Bessel functions, which have well-studied properties. The performance predicted by our model matches closely with that obtained using a widely-used circuit simulator. This model provides an important building block for further system-level performance analysis and optimization to address the increasing demand to extend the operation range and/or reduce cost and size of state-of-the-art self-powered wireless sensors.

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