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Theoretical Model For Maximum Throughput of a Radio Receiver with Limited Battery Power

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***Abstract*— Maximizing the battery life time of mobile devices and sensor nodes increasingly becomes a challenge. In many applications the energy consumed by the receiver is orders of magnitude larger than the energy consumed by the transmitter. We address the challenge of achieving the highest possible throughput per Watt of available receiver circuit power. Our closed form solution allows us to formalize the relation between adjacent channel interference power and achievable throughput for a given available receiver circuit power budget. We conclude that for a given adjacent channel interference level, there is an optimum receiver power that needs to be applied to operate the link at optimum efficiency in terms of bits per Joule. If the receiver has less power available than this optimum, it preferably applies a duty cycling scheme, switching between an off state and operation at the optimum power. This observation is contrast to commonly used capacity models where throughput is limited by *transmit* power.**

I. Introduction

Receiver power consumption tends to become more problematic than delivering adequate transmit power, when maximizing battery life time of mobile devices and sensor nodes. In many applications, the mobile user spends significantly more time receiving data than transmitting. Often, the energy consumed in receiving mode is several orders of magnitude larger than the energy consumed in transmit mode [1] [2], even if the transmitter circuit power consumption is larger than the receiver circuit power consumption when switched on. Secondly, in a short range link, the transmit power can be relatively small. So the transmit power amplifier is no longer the main power consumer. Yet, the receiver front end often needs to recover a weak signal in the presence of strong adjacent channel interference, which requires highly linear, thus power hungry radio frequency (RF) designs. In the absence of disruptive new approaches, we expect that this trend will continue for the foreseeable future.

A commonly used direct-conversion receiver architecture is used in our analysis. In most receivers a broad band signal is processed at radio frequency (RF) by the analog front end, where the desired signal only occupies a small portion of the front-end bandwidth. To present the desired signal to the baseband (BB) ADC, the analog front end amplifies, down-converts, and filters the received RF broadband signal. Therefore, the first stages of our receiver usually contains strong adjacent channel interferers, with a priori not fully known statistical properties [3]. These signals need to be handled with adequate linearity to avoid excessive distortion spill-over into the band of the desired signal [4].

In [5] a top down approach for RF receiver power minimization is proposed to cope with the typical complexity of RF circuit blocks. In the proposed approach characteristics of the RF stages such as linearity, gain, bandwidth, and circuit power consumption can be interchanged via structurally independent transforms (SIT), independent of circuit topology, IC process, lay out, and so on [6]. Designs for stages are ranked according to their power efficiency via an effective figure of merit (EFOM), which does depend on circuit topology, IC process, lay out, and so on. The approach minimizes the total circuit power of the receiver cascade by optimally interchanging the characteristics of the stages via the SIT. Therefore the abstract optimum is independent of circuit topology, IC process, lay out and so on. By selecting the best EFOMs for each stage from a circuit library and using SIT the chosen circuit topology for a stage can be transformed to correspond to the optimal specification. This approach was illustrated for a cascade of two stages in [7].

From recent insights in IC design optimizations [8], we conclude that the most dominant factor in power consumption for low power designs is the linearity requirement (in terms of the third order intercept point (IP3)). The optimum system specifications for the receiver cascade that are derived, also lead to specification for the IP3, noise figure (NF) and gain of individual stages. Our closed form solution allows us to formalize the relation between adjacent channel interference power and achievable throughput for a given available receiver circuit power budget. Therefore, the theory links the highest achievable number of bits per Joule in a given IC technology to adjacent channel interference robustness.

The optimum appears to depend mainly on the strength of adjacent channel interference. Furthermore, the throughput as a function of the receiver circuit power budget observes an optimum. Too low receiver circuit power would lead to a highly non-linear receiver, hence strong distortion and low throughput. Too high values of receiver circuit power would create an unnecessarily linear receiver, which cannot be exploited because of the finite signal-to-channel-noise ratio of the received signal. A main contribution of this paper is that for very low available receiver circuit power, our results imply that a duty cycle strategy is more efficient than continuous

operation. The receiver is proposed to operate in bursts. This observation is contrast to commonly used capacity models where throughput is limited by *transmit* power. In such models the link capacity appeared insensitive to the chosen waveform, but merely determined by E_b/N_0. In modern short range low power systems, receiver power is a more severe limitation, and new models are required. This paper contributes to the formulation of these.

II. Modeling System Throughput Efficiency

This text has previously been published in a different version in [8]. However, it is included in this paper to provide the reader with the necessary steps of the derivation.

To operate a wireless network at the highest efficiency possible for a given receiver circuit power budget with $\sum P_m = P_r$ we strive to find

$$\widehat{T} = \max T \,|_{\sum P_m = P_r}, \tag{1}$$

here P_m is the power allocated to the m^{th} stage of a receiver circuit. The maximum is taken over all possible settings of the RF stages, provided that the total consumed power does not exceed P_r. We use the capacity expression

$$T = \log_2\left(1 + \frac{S}{N_{tot}}\right) \tag{2}$$

as a measure of achievable throughput T. Here S is the input signal power. Yet, T should not be interpreted as the Shannon capacity of the system in information theoretic sense: if the sampling and ADC circuits are allowed to capture the entire band, including the interference signal, the distortion can be predicted by the BB DSP and its effect can be eliminated, at least from an information theoretical perspective. Hence one could design a receiver that has higher throughput than the value found in (2). However, such a receiver architecture would be at odds with our ambition to minimize the receiver circuit power consumption. Lacking a better model, we define the throughput T as in (2). The total noise plus distortion, relative to power levels at the input, is

$$N_{\text{tot}} = N_{th} + \frac{N_r}{G_{\text{tot}}} + \frac{N_d}{G_{\text{tot}}}, \tag{3}$$

where N_{th} is the noise in the channel, N_r the electronics noise added by the analog circuits of the receiver, and N_d is the distortion caused by an interferer. Other RF impairments such as LO leakage, DC leakage and images are not considered, since they are related to the architecture, topology and layout, which are beyond the scope of this paper. The AWGN noise in the channel is given by $N_{th} = kTB$. where $k = 1.38 \times 10^{-23}$ is Boltzmann's constant, T is the temperature and B is the bandwidth of the desired signal. Further, G_{tot} is the total maximum power gain of the analog receiver given by

$$G_{\text{tot}} = \prod_{m=1}^{M} G_m, \tag{4}$$

where G_m is the gain of the m^{th} stage in the cascade (Figure 1). We now need a more detailed model of N_d and N_r.

A. Distortion and Noise

The distortion is expressed as [8]

$$N_d = \frac{G_{\text{tot}} P_{int}^3}{IP3_{\text{tot}}^2}. \tag{5}$$

Here $IP3_m$ is the third order intercept point of the m^{th} stage. We simplify our model by assuming that, after further channel selectivity filtering, Nyquist sampling and A/D conversion, the baseband processing engine of the receiver has no further knowledge of this distortion signal, and experiences it as AWGN [9]. The total worst case $IP3$ of M stages can be calculated via [5]

$$IP3_{\text{tot}} = \left(\sum_{m=1}^{M} \frac{\prod_{j=1}^{m-1} G_j}{IP3_m}\right)^{-1}, \tag{6}$$

under the worst case assumption that all distortion components are in-phase.

Next to the distortion signals, the analog front end adds noise N_r to the desired signal. This addition of noise is modeled via the noise figure (NF), and is defined as NF$= 10\log_{10}(F_m)$. Here, the noise factor F_m is defined as:

$$F_m = \frac{\text{SNR}_m}{\text{SNR}_{m+1}}, \tag{7}$$

where SNR_m is the SNR at the input, and SNR_{m+1} is the SNR at the output of the m^{th} stage in a cascade. Note that the noise figures do not model the contribution by distortion. The total noise-factor of M stages in a cascade, F_{tot}, can be calculated via Friis forumula

$$F_{\text{tot}} = 1 + \sum_{m=1}^{M} \frac{F_m - 1}{\prod_{j=1}^{m-1} G_j}, \tag{8}$$

where F_m the noise-factor of the m^{th} stage and G_j the gain of the j^{th} stage. Moreover, the total noise factor must satisfy

$$F_{\text{tot}} = 1 + \frac{N_r}{G_{\text{tot}} N_{th}} \tag{9}$$

where G_{tot} is the total gain of the analog circuit and N_r is the variance of the electronics noise added by all analog circuits weighed with the partial gains. The electronics noise can now be expressed as

$$N_r = (F_{tot} - 1)\, N_{th} G_{tot} \tag{10}$$

By combining (3) (5) and (10), the total noise plus distortion, normalized to power levels present at the input, is now given by

$$N_{\text{tot}} = F_{\text{tot}} N_{th} + \frac{P_{int}^3}{IP3_{\text{tot}}^2}, \tag{11}$$

where $IP3_{tot}$ follows from (6) and F_{tot} from (8). Figure 1 now depicts the receiver model, where every individual stage has variable gain ($G_1, \cdots, G_M$) and IP3 ($IP3_1, \cdots, IP3_M$), thus allowing for variable $IP3_{tot}$ and variable F_{tot} of the receiver cascade.

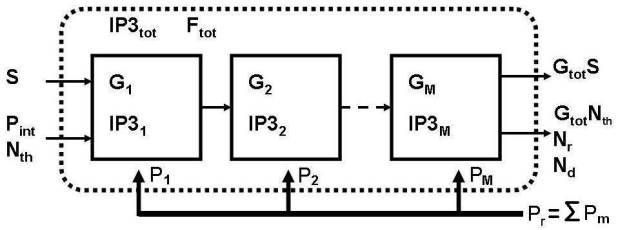

Fig. 1: *Power consumption P_r in a receiver, to be optimized by adapting the $IP3$ and Gain G of each of the M stages.*

B. Optimum Throughput

In [8] our aim is to optimize the power budget P_r over the various stages such that throughput T is optimum under the constraint of a given technology, a given received power S, total gain G_{tot} needed to drive the ADC and channel parameters N_{th} and P_{int}. A commonly encountered design problem in RF design is that of optimizing each circuit block to meet a given spec for the total receiver. So for a chosen F_{tot} and $IP3_{\text{tot}}$ one needs to optimize the power budget P_r by optimally distributing the gains $(G_1,\ \cdots,\ G_M)$ and $IP3$'s $(IP3_1,\ \cdots,\ IP3_M)$ over the cascade. In [5] a double Lagrangian tool is proposed for this exercise, to solve the distribution of the gains and $IP3$ for the cascade. Paper [7] summarizes [5] for $M = 2$. This Minimum Power Cascade Optimization (MPCO) solves:

$$P_{\text{min}} = \min\left(\sum_{m=1}^{M} P_m\right), \tag{12}$$

where P_m is the power dissipation of circuit block m, as will be covered by (15). In [8] we extend the MPCO by further optimizing F_{tot} and $IP3_{\text{tot}}$ to satisfy our end goal of maximizing the throughput, thus searching for

$$\widehat{T} = \max_{F_{\text{tot}},\, IP3_{\text{tot}}} (T), \tag{13}$$

where the available receiver circuit power P_r, satisfies $P_r = P_{min}$ as in (12). This is achieved by expressing the power optimal $IP3_{\text{tot}}$, called $\widehat{IP3}_{\text{tot}}$, as a closed form function (20) of the figure of merits related to the used IC design process, the available receiver circuit power P_r, the power optimal total noise factor $\widehat{F}_{\text{tot}}$ and total gain G_{tot}. Therefore, we can write N_{tot} as a function of $\widehat{F}_{\text{tot}}$ and the available receiver circuit power P_r. Our claim is that in the end the maximization in (13), for a given power budget P_r, is equal to minimizing the total noise according to

$$\widehat{N}_{\text{tot}} = \min_{F_{\text{tot}}} \left(N_{tot}\left(\widehat{IP3}_{\text{tot}}(F_{\text{tot}})\right)\right). \tag{14}$$

We call this a Maximum Throughput Cascade Optimization Method (MTCO).

C. Minimum Power Cascade Optimization Method

1) Linearity Factor Model: A commonly used equivalent figure of merit (EFOM) [5] is

$$P_m = \frac{f_m G_m\ IP3_m}{\kappa_m}, \tag{15}$$

where f_m is the power limiting bandwidth and κ_m is the power linearity factor of the m^{th} stage. The most appropriate parameter to choose for f_m highly depends on the circuit functionality. For LNAs with a dominant pole, the bandwidth is an appropriate choice. By using an EFOM, P_m theoretically does not depend on the noise figure F_m. By using structure independent transforms (SIT), it is possible to trade IP3, gain and power dissipation, to transform a chosen topology for each circuit block to a circuit with the optimal specification [6]. Creating a topology that can also change $IP3$ adaptively and stil meet (15) is a topic of current IC design research.

2) Dual Lagrange Optimization Method: So,

$$P_{\text{min}} = \min_{\substack{G_1,\ \cdots,\ G_M \\ IP3_1,\ \cdots,\ IP3_M}} \left(\sum_{m=1}^{M} \frac{f_m}{\kappa_m} G_m\ IP3_m\right), \tag{16}$$

while achieving the G_{tot} using (4), $IP3_{\text{tot}}$ using (6), and F_{tot} using (8). In this optimization process, the f_m, κ_m and F_m of a cascade are taken as constant. The individual F_m is kept constant because the F_m is limited by the topology and used IC process technology. A closed form expression [5] for the minimal analog signal conditioning (ASC) power dissipation as a function of the overall noise factor F_{tot} is,

$$P_{\text{min}} = IP3_{\text{tot}}\left(\sqrt{F_e} + \sqrt{\frac{F_w}{(F_{\text{tot}} - F_1)}}\right)^2, \tag{17}$$

where the "weighed excess noise factor" F_w is defined as

$$F_w = \left(\sum_{m=1}^{M-1} \sqrt[3]{\frac{f_m}{\kappa_m}(F_{m+1} - 1)}\right)^3. \tag{18}$$

Here the excess noise factor of the final stage is

$$F_e = \frac{f_M}{\kappa_M} G_{\text{tot}}, \tag{19}$$

which is a fixed value.

D. Maximum Throughput Cascade Optimization Method

While (17) gives the minimum power P_{min} needed to satisfy a required $IP3_{tot}$, we can conversely claim that the best $\widehat{IP3}_{\text{tot}}$ that one can achieve for a given available P_r equals

$$\widehat{IP3}_{\text{tot}} = P_r\left(\sqrt{F_e} + \sqrt{\frac{F_w}{(F_{\text{tot}} - F_1)}}\right)^{-2}. \tag{20}$$

Now, we can rewrite the total noise (3) as a function depending on F_{tot}, P_{int} and P_r

$$N_{\text{tot}} \quad = F_{\text{tot}} N_{th} + \frac{P_{int}^3}{P_r^2}\left(\sqrt{F_e} + \sqrt{\frac{F_w}{(F_{\text{tot}} - F_1)}}\right)^4, \tag{21}$$

By combining (1), (2), (3), and (21), we can maximize T by minimizing N_{tot}. We require that

$$\left.\frac{dN_{\text{tot}}(F_{\text{tot}})}{dF_{\text{tot}}}\right|_{F_{\text{tot}}=\widehat{F}_{\text{tot}}} = 0, \tag{22}$$

and obtain $\widehat{F}_{\text{tot}}$ as $\widehat{F}_{\text{tot}} =$

$$F_1 + \frac{4F_w}{\left(-\sqrt{F_e} + \sqrt{F_e + 2^{5/3}\left(F_w N_{th}\frac{P_r^2}{P_{int}^3}\right)^{1/3}}\right)^2}. \tag{23}$$

Applying this value of $\widehat{F}_{\text{tot}}$ means that (10) turns into $N_r/G_{\text{tot}} =$

$$(\mathrm{F}_1 - 1)\, N_{th} + \frac{4F_w N_{th}}{\left(-\sqrt{F_e} + \sqrt{F_e + 2^{5/3}\left(F_w N_{th}\frac{P_r^2}{P_{int}^3}\right)^{1/3}}\right)^2}, \tag{24}$$

and (5) turns into $N_d/G_{\text{tot}} =$

$$\frac{P_{int}^3}{P_r^2}\frac{1}{16}\left(\sqrt{F_e} + \sqrt{F_e + 2^{5/3}\left(F_w N_{th}\frac{P_r^2}{P_{int}^3}\right)^{1/3}}\right)^4, \tag{25}$$

which we insert in (2) and (3). We now have found an analytically closed-form solution which maximizes the throughput for a given circuit power budget P_r. We also found closed-form solutions for $\widehat{F}_{\text{tot}}$ and $\widehat{IP3}_{\text{tot}}$ that achieve the optimum throughput, respectively (23) and (20) with (23) inserted. The individual gain $(G_1, \cdots, G_M)$ and $IP3$ $(IP3_1, \cdots, IP3_M)$ per stage follow from [5]. In Section III we give an example of MPCO to motivate our search for the MTCO, calculating the efficiency in terms of bits/Joule for a target $NF_{tot} = 2$ dB, with first $IP3_{tot} = -40$ dBm, and secondly $IP3_{tot} = -20$ dBm. Surprisingly, in our scenario, the efficiency at $IP3_{tot} = -40$ dBm is more than an order of magnitude larger than at $IP3_{tot} = -20$ dBm, namely 4.4 Gbit/Joule and 0.3 Gbit/Joule, respectively. The difference in P_r is 8 dBm (5.9 mW) versus 28 dBm (590 mW), respectively.

E. Duty Cycling

Interestingly, the maximum efficiency for a given receiver circuit power in terms of bits per Joule observes an optimum as depicted in Figure 3. At the left hand side of the optimum, very low receiver circuit power leads to a highly non-linear receiver, causing strong distortion and spill over of adjacent channel interferers, thus limiting the throughput. At the right hand side of the optimum the receiver can not effectively exploit the availability of more receiver circuit power, because the link capacity is limited by E_b/N_0.

A strategy to operate at the optimal efficiency and to achieve lower average power consumption is duty cycling. The receiver operates at the optimal efficiency and switches on and off according to the available circuit power. Via (2), (3), (24), and (25) the throughput which corresponds to the maxima of the curves in Figure 3 is calculated. Interestingly, the optimum throughput is independent of the CIR. However, the receiver circuit power required to achieve this throughput is not (Figure 4). The MTCO now allows us to determine when duty cycling is an appropriate strategy when maximizing battery life time.

However, in systems with very short duty cycles, the overhead for short packages can be prohibitive. In such cases there exists a tradeoff between the delay for merging packets versus the optimal power consumption. Furthermore, at the right hand side of the optimum, the throughput T expressed in bit/s/Hz can increase by making more circuit power available. However, the throughput BT/P_r expressed in bits/Joule cannot increase if a more power consuming circuit is used. Designing for better linearity than does not pay off

TABLE I: *κ_m for various LNA circuit designs in 90 nm CMOS.*

LNA	[10]	[11]	[12]	[13]	[13]
NF [dB]	3.4	4.4	1.7	2.0	3.0
BW [GHz]	4.1†	19.9	1.5	6.0†	4.0†
Gain [dB]	12.4	12.7	16	15	14
IIP3 [dBm]	-1	-2.5	4.0	-2.3	5.6
Pdc [mW]	9.0	12.6	19.6	19.2	19.2
κ_m [10^9]	6.50	18.0	7.65	6.01	19.0
LNA	[14]	[15]	[16]	[17]	[18]
NF [dB]	4.4	2.1	2.9	3.6	6.5
BW [GHz]	5†	0.6†	1.35	1.14	8
Gain [dB]	13.5	13.4	12.3	8.1	14.1
IIP3 [dBm]	-8‡	-10	-2.7	-7.25	-1.7‡
Pdc [mW]	4.0	1.2	9.72	1.0	86
κ_m [10^9]	4.91	1.18	1.33	1.48	1.62

† Estimated from the calculated maximum Power Gain.
‡ Estimated from the 1 dB compression point.

TABLE II: *κ_m for various Mixer circuit designs in 90 nm CMOS.*

Mixer	[19]	[20]†	[21]
NF [dB]	17.4	11.5	9.1
f_m **[GHz]**	20	3.85	2.1
Gain [dB]	3.2	12.1	10.2
IIP3 [dBm]	-2.1	-2.8‡	10.7
Pdc [mW]	1.8	9.78	14.5
κ_m	$14.3{\cdot}10^9$	$3.35{\cdot}10^9$	$17.8{\cdot}10^9$

† Merged Mixer and LNA.
‡ Estimated from the 1 dB compression point.

TABLE III: *κ_m for various Output buffer circuit designs in 90 nm CMOS.*

Buffer	[22]	[23]	[24]
NF [dB]	16	26.5‡	25
f_m **[MHz]**	500	10	2
Gain [dB]	0	67.5†‡	14†
IIP3 [dBm]	19	-52.5	-4
Pdc [mW]	32.5	13.3	1
κ_m	$1.22{\cdot}10^9$	$2.37{\cdot}10^7$	$2.00{\cdot}10^7$
Buffer	[25]	[26]	[26]
NF [dB]	12.3‡	17	30
f_m **[MHz]**	0.24	2200	2200
Gain [dB]	33†	-10†	50†
IIP3 [dBm]	-18	-3	-45
Pdc [mW]	23.8	2.5	2.5
κ_m	$3.19{\cdot}10^5$	$4.40{\cdot}10^7$	$2.78{\cdot}10^9$

† Voltage gain.
‡ Estimated from data.

III. Numerical Results

We first start with an example of the traditional Minimum Power Cascade Optimization (MPCO), and show how this can lead to a non-optimum system in terms of throughput per Joule. From our circuit library in Table I, II, and III, we select the circuits with the best EFOM to Table IV. As an example

TABLE IV: *Typical design choices for cascades in an ASC (LNA [12], Mixer [21], and Output buffer [22]). Where, numbers denoted in italics are considered as variable in this paper.*

	LNA	Mixer	Buffer
NF [dB]	1.7	9.1	16
Gain [dB]	*16*	*10.2*	*0*
IIP3 [dBm]	*4*	*10.7*	*19*
κ_m	$7.65{\cdot}10^9$	$17.8{\cdot}10^9$	$1.22{\cdot}10^9$
f_m **[MHz]**	100	2500	22

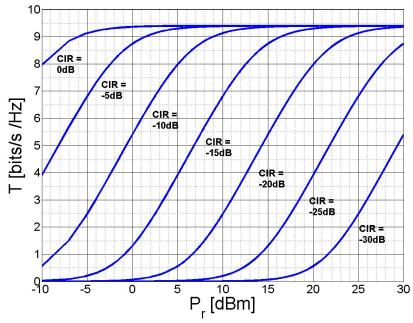

Fig. 2: *Achievable Throughput (bit/s/Hz) for different values of CIR due to adjacent channel interference, versus available receiver circuit power P_r for a WLAN-like system in 90nm CMOS.*

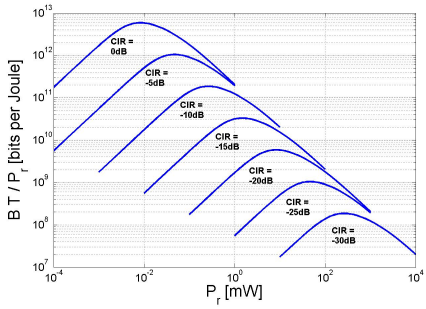

Fig. 3: *Bits per Joule for different values of CIR due to adjacent channel interference, versus receiver circuit power P_r for a WLAN-like system in 90nm CMOS.*

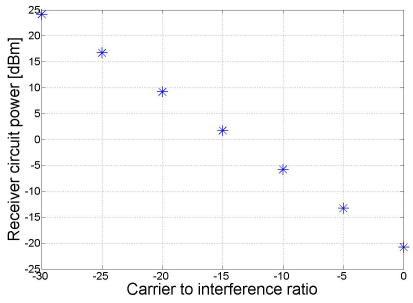

Fig. 4: *Optimal receiver circuit power to be allocated to the receiver for maximum throughput efficiency (in bits/J) for different values of adjacent channel interference, for a WLAN-like system in 90 nm CMOS with SNR = 30dB,.*

the target specifications for the MPCO are $NF_{tot} = 2$ dB, with first $IP3_{tot} = -40$ dBm, and secondly $IP3_{tot} = -20$ dBm. We consider a transmitter that can provide ample S/N_{th}, namely of 30 dB. Adjacent channel interference is at + 20 dB, i.e., CIR $= -20$ dB. We use the EFOM of Table IV for 90 nm CMOS. Further, $T = 295$ K, $G_{tot} = 65$ dB. The characteristic frequencies f_m are chosen to satisfy the frequency requirements of an IEEE802.11b system in the 2.4 GHz band, with $B = 22$ MHz, f_m is for the LNA $f_1 = 100$ MHz, the mixer $f_2 = 2500$ MHz, and the output buffer $f_3 = 22$ MHz. The MPCO gives the power needed to operate this receiver. The result is very illustrative: The efficiency for a system operating at $IP3_{tot} = -40$ dBm is 4.4 Gbit/Joule ($T = 1.1$ bits/s/Hz, $P_r = 8$ dBm), and at $IP3_{tot} = -20$ dBm it is 0.3 Gbit/Joule ($T = 9.2$ bits/s/Hz, $P_r = 28$ dBm). This motivated our search for a MTCO which results in the optimal setting for NF_{tot} and $IP3_{tot}$ in terms of maximizing the throughput per unit of receiver circuit power.

The closed-form solution for optimum throughput as a function of available receiver circuit power and for various values of CIR is depicted in figure 2, using (2), (3), (24) and (25). For large available receiver power the throughput approaches the throughput for a signal 30 dB above thermal noise, and for an LNA with noise figure $F_1 = 1.7$ dB. At small available receiver power N_r and N_d become dominant. The figure shows that when the CIR is decreased, more power is needed to achieve a certain throughput. The closed-form solution for maximizing throughput can be extended to express bits per Joule as a function of available receiver power BT/P_r, using (1), (2), (3), (24) and (25). The result is depicted in Figure 3. When the CIR is decreased, the efficiency in bits per Joule for a given available receiver power is decreased as well.

IV. Conclusions

For a given adjacent channel interference level, there is an optimum receiver power that needs to be applied to operate the link at optimum efficiency in terms of bits per Joule. If the receiver has more power available, it can not effectively exploit this because the link capacity is limited by E_b/N_0. If the receiver has less power available than this optimum, it preferably applies a duty cycling scheme, switching between an off state and operation at the optimum power. This observation is contrast to commonly used capacity models where throughput is limited by *transmit* power. In such models the link capacity appeared insensitive to the chosen waveform, but merely determined by E_b/N_0. In modern short range low power systems, receiver power is a more severe limitation.

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References

[1] J. Liu and L. Zhong, "Micro Power Management of Active 802.11 Interfaces," *MobiSys08*, June 2008.

[2] R. Krashinsky and H. Balakrishnan, "Minimizing Energy for Wireless Web Access with Bounded Slowdown," *MOBICOM02*, Sep 2002.

[3] D. Cabric, M. S. Chen, D. A. Sobel, S. Wang, J. Yang, , and R. Brodersen, "Novel Radio Architectures for UWB, 60 GHz, and CognitiveWireless Systems," *EURASIP Journal on Wireless Communications and Networking, Special Issue on CMOS RF Circuits for Wireless Applications*, vol. 2006, Apr 2006.

[4] B. Razavi, "Challenges in Portable RF Transceiver Design," *Circuits and Devices Magazine, IEEE*, vol. 12, no. 5, 1996.

[5] P. Baltus, *Minimum Power Design of RF Front Ends*. PhD thesis, Eindhoven University of Technology, September 2004. http://library.tue.nl/catalog/LinkToVubis.csp?DataBib=6:580521.

[6] P. Baltus, "Put your power into SOA LNAs!," *Workshop on Advances in Analogue Circuit Design*, 1998.

[7] P. Baltus and R. Dekker, "Optimizing RF Front Ends for Low Power," *Proceedings of the IEEE*, vol. 88, pp. 1546–1559, Oct 2000.

[8] J. van den Heuvel, J.-P. Linnartz, and P. Baltus, "Optimizing Throughput for Limited Receiver Circuit Power," *IEEE International Symposium on Circuits and Systems 2010, ISCAS 2010*, May 2010.

[9] S. Verdú, "Spectral Efficiency in the Wideband Regime," *IEEE Transactions on Information Theory*, vol. 48, pp. 1319–1343, June 2002.

[10] D. Linten, S. Thijs, W. Jeamsaksiri, J. Ramos, A. Mercha, M. Natarajan, P. Wambacq, A. Scholten, and s. Decoutere, "An Integrated 5 GHz Low-Noise Amplifier with 5.5 kV HBM ESD Protection in 90 nm RF CMOS," *VLSI Circuits, 2005. Digest of Technical Papers. 2005 Symposium on*, pp. 86–89, June 2005.

[11] M. Chen and J. Lin, "A 0.1-20 GHz Low-Power Self-Biased Resistive-Feedback LNA in 90 nm Digital CMOS," *Microwave and Wireless Components Letters, IEEE*, vol. 16, pp. 323–325, May 2009.

[12] L. Aspemyr, H. Sjoland, H. Jacobsson, M. Bao, and G. Carchon, "A 5.8 GHz 1.7 dB NF Fully Integrated Differential Low Noise Amplifier in CMOS," *Microwave Conference, 2006. APMC 2006. Asia-Pacific*, pp. 309–312, Dec 2006.

[13] L. Aspemyr, H. Jacobsson, M. Bao, H. Sjoland, M. Ferndahl, and G. Carchon, "A 15 GHz and a 20 GHz Low Noise Amplifier in 90 nm RF-CMOS," *Silicon Monolithic Integrated Circuits in RF Systems, 2006. Digest of Papers. 2006 Topical Meeting on*, Jan 2006.

[14] E. Cohen, S. Ravid, and D. Ritter, "An Ultra Low Power LNA with 15dB Gain and 4.4dB NF in 90nm CMOS Process for 60 GHz Phase Array Radio," *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE*, pp. 61–64, Apr 2008.

[15] D. Linten, X. Sun, S. Thijs, M. Natarajan, A. Mercha, G. Carchon, P. Wambacq, T. Nakaie, and S. Decoutere, "Low-Power Low-Noise Highly ESD Robust LNA, and VCO Design Using Above-IC Inductors," *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*, pp. 497–500, Sep 2005.

[16] D. Linten, S. Thijs, M. Natarajan, P. Wambacq, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Donnay, and S. Decoutere, "A 5 GHz Fully Integrated ESD-Protected Low-Noise Amplifier in 90 nm RF CMOS," *Solid-State Circuits Conference, 2004. ESSCIRC 2004. Proceeding of the 30th European*, pp. 291–294, Sep 2004.

[17] D. Linten, L. Aspemyr, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Thijs, R. Garcia, H. Jacobsson, P. Wambacq, S. Donnay, and S. Decoutere, "Low-Power 5 GHz LNA and VCO in 90 nm RF CMOS," *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on*, pp. 372–375, Jun 2004.

[18] S. Pellerano, Y. Palaskas, and K. Soumyanath, "A 64 GHz LNA With 15.5 dB Gain and 6.5 dB NF in 90 nm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 43, pp. 1542–1552, Jul 2008.

[19] C. Kienmayer, M. Tiebout, W. Simburger, and A. Scholtz, "A Low-Power Low-Voltage NMOS Bulk-Mixer with 20 GHz Bandwidth in 90 nm CMOS," *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on*, vol. 4, pp. 385–388, May 2004.

[20] A. Amer, E. Hegazi, and H. F. Ragaie, "A 90-nm Wideband Merged CMOS LNA and Mixer Exploiting Noise Cancellation," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 323–328, Feb 2007.

[21] S. Peng, C.-C. Chen, and A. Bellaouar, "A Wide-Band Mixer for WCDMA/CDMA2000 in 90nm Digital CMOS Process," *Radio Frequency integrated Circuits (RFIC) Symposium, 2005. Digest of Papers. 2005 IEEE*, pp. 179–182, Jun 2005.

[22] T. Hui Teo, M. W. G. Y. Annamalai Arasu, and M. Itoh, "A 90nm CMOS Variable-Gain Amplifier and RSSI Design for Wide-Band Wireless Network Application," *Solid-State Circuits Conference, 2006. ESSCIRC 2006. Proceedings of the 32nd European*, pp. 86–89, Sep 2006.

[23] M. Elmala, B. Carlton, R. Bishop, and K. Soumyanath, "A 1.4V, 13.5mW, 10/100MHz 6th Order Elliptic Filter/VGA with DC-Offset Correction in 90nm CMOS [WLAN Applications]," *Radio Frequency integrated Circuits (RFIC) Symposium, 2005. Digest of Papers. 2005 IEEE*, pp. 189–192, Jun 2005.

[24] N. Stanic, A. Balankutty, P. Kinget, and Y. Tsividis, "A 2.4-GHz ISM-Band Sliding-IF Receiver With a 0.5-V Supply," *Solid-State Circuits, IEEE Journal of*, vol. 43, pp. 1138–1145, May 2008.

[25] N. Stanic, A. Balankutty, P. Kinget, and Y. Tsividis, "Low-IF 90nm CMOS Receiver for 2.5G Application," *Electrotechnical Conference, 2004. MELECON 2004. Proceedings of the 12th IEEE Mediterranean*, vol. 1, pp. 151–154, May 2004.

[26] Y. Wang, B. Afshar, T.-Y. Cheng, V. Gaudet, and A. Niknejad, "A 2.5mW Inductorless Wideband VGA with Dual Feedback DC-Offset Correction in 90nm CMOS Technology," *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE*, pp. 91–94, Apr 2008.